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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,696	02/11/2000	Donald J. Urbas	068856/221	5539

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EXAMINER	
YANG, CLARA I	

ART UNIT	PAPER NUMBER
2635	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/502,696	Applicant(s) URBAS ET AL.	
	Examiner Clara Yang	Art Unit 2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *17-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 41-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *05* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 17 - 40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 04.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 - 4, 6 - 8, 10, 11, 13, 15, 16, and 41 - 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Urbas et al. U.S. Patent No. 5,767,792.

Referring to Claims 1 and 7, as shown in Fig. 1, Urbas' transponder comprises: (a) an EEPROM 25 with 16 addressable bytes for storing data (see Col. 1, lines 51 - 52 and 61 - 65; and Col. 7, lines 53 - 54); (b) an address and timing generator 23 for outputting an OUTPUT ENABLE (or read) signal via data sequence generator 26 and a WRITE ENABLE (or program) signal via programming timing generator 80, wherein both signals supply current to EEPROM 25 26 (see Col. 7, lines 54 - 64 and Col. 14, lines 8 - 51); (c) a divider 70*b* (see Fig. 2) or address module for addressing an address in EEPROM 25 in response to a clock signal from address and timing generator 23 (see Col. 4, lines 59 - 67 and Col. 5, lines 1 - 11); (d) a data bus 30 and a universal shift register 11 for receiving the data stored in EEPROM 25 at an address indicated by address and timing generator 23 and for inputting data into EEPROM 25 (see Col. 7, lines 63

- 65; Col. 8, lines 1 - 10; and Col. 14, lines 1 - 12). Here it is understood that: (a) divider 70*a* of address and timing generator 23 (see Fig. 2), data sequence generator 26, and programming timing generator 80 form a clock generator; and (b) data bus 30 and universal shift register 11 form a data module. Urbas teaches that data sequence generator 26 low tri-states (i.e. stops supplying current) the output of EEPROM 25 once its data has been output to the data module as to avoid conflicting with data from buffer 9 and multiplexer 9A (see Col. 7, lines 57 - 60).

Regarding Claim 2, Urbas teaches that the A_0-A_3 outputs (or address clock signal) of divider 70*b* are used to sequentially address the bytes of EEPROM 25 via address bus 28 (see Col. 5, lines 3 - 6). Here it is understood that each address clock signal is increased sequentially by divider 70*b* in order to change the address of EEPROM 25 as identified by address and timing generator 23. Address and timing generator 23 also sends a signal to data sequence generator 26 (see Fig. 1) that causes data sequence generator 26 to produce a high OUPUT ENABLE signal to EEPROM 25, thus permitting EEPROM 25 to output its data (see Col. 7, lines 53 - 67). Here it is understood that a high OUTPUT ENABLE signal provides a supply current to EEPROM 25.

Regarding Claim 3, as shown in Fig. 1, Urbas' clock generator outputs (a) a WRITE ENABLE signal or program signal that supplies current to EEPROM 25 in order to program EEPROM 25 (see Col. 14, lines 8 - 12 and 33 - 51); and (b) an address clock signal or latch signal (see Col. 4, lines 59 - 64). In response to the address latch signal the clock generator, divider 70*b* (or address module) selects a specific address of EEPROM 25 (see Fig. 2, divider 70*b*, outputs A_0-A_3; and Col. 5, lines 3 - 8). The data module inputs data into memory at the address indicated by the address module (see Col. 13, lines 61 - 67 and Col. 14, lines 1 - 12). Once the data in the data module has been stored in memory, the clock generator stops sending the

WRITE ENABLE signal, thus turning off EEPROM 25 and allowing the transponder to resume transmission of the RECEIVE CLOCK signal to the interrogator (see Col. 14, lines 52 - 59).

Regarding Claims 4 and 8, Urbas' transponder has an EEPROM 25 with 16 addressable bytes (see Col. 7, lines 53 - 56). Because sequence generator 26 determines from the 8th data bit of the 16th byte whether or not to allow mode decoder 27 to look for a command sequence that places the transponder in the program mode (see Col. 6, lines 7 - 13), it is understood that the 16th byte is a status byte region and that the remaining 15 bytes form the data region of EEPROM 25 and that data sequence generator 26 and mode decoder 27 form a program control. Urbas discloses that once the transponder is in the program mode, the clock generator outputs the WRITE ENABLE signal to the programming timing generator 80, thus starting the write cycle and causing the data received from the interrogator to be written to EEPROM 25 at the desired address (see Col. 6, lines 31 - 44).

Regarding Claims 6 and 10, Urbas imparts that the if the 8th data bit of EEPROM 25's 16th byte is set to logic 1 and that the transponder's power level is adequate for programming, the transponder enters the programming mode and writes the data on data bus 30 to the desired address of EEPROM 25. If the 8th data bit of EEPROM 25's 16th byte is cleared or set to logic 0, the transponder is prevented from entering the programming mode. (See Col. 6, lines 7 - 13 and 31 - 49.) Here it is understood that the 8th data bit of EEPROM 25's 16th byte is an HLOCK bit.

Regarding Claim 11, Urbas teaches that when a transponder receives sufficient power from an interrogator, the transponder enters the program mode after receiving three predetermined pulses from the interrogator (see Col. 12, lines 42 - 53). Because the three pulses must be received by the transponder within a predetermined time window (i.e. during the

transmission of EEPROM 25's 16th byte of data), it is understood that the three pulses are pulse space modulated. Furthermore, because Urbas expresses that a user can specify any address of EEPROM 25 to be written to (see Col. 15, lines 1 - 12) and that the master clock is disabled during the write cycle to prevent the clock generator for selecting the next address (see Col. 14, lines 42 - 45), it is implied that the clock generator supplies an address latch signal once an interrogator transmits three pulses to change the transponder's operation mode from read to program, a first byte of data, and a 9th bit indicating that the data is to be written to that specific address.

Referring to Claim 13, Urbas' transponder, as shown in Fig. 1, has the following: (a) EEPROM 25 with 16 addressable bytes, wherein the 16th byte is understood to be a status byte as explained above in Claims 4 and 8; (b) an address and timing generator 23 for receiving a program signal from mode decoder 37 and for outputting a data latch signal (or WRITE ENABLE signal) that causes programming timing generator 80 to start the write cycle and to have the data in shift register 11 written to EEPROM 25 (see Col. 6, lines 31 - 44); (c) a divider 70*b* or address module for receiving an address latch signal from divider 70*a* and addressing a predetermined address in EEPROM 25 to be programmed (see Col. 4, lines 54 - 64; Col. 5, lines 3 - 6; and Col. 13, lines 1 - 12); and (d) data sequence generator 26 and mode decoder 27 for reading the status byte and outputting a program enable signal in response to the 8th data bit (see Col. 6, lines 7 - 13). Here it is understood that data sequence generator 26 and mode decoder 27 form a program control.

Regarding Claim 15, Urbas imparts that the if the 8th data bit of EEPROM 25's 16th byte is set to logic 1 and that the transponder's power level is adequate for programming, the transponder enters the programming mode and writes the data on data bus 30 to the desired

address of EEPROM 25. If the 8th data bit of EEPROM 25's 16th byte is cleared or set to a logic 0, the transponder is prevented from entering the programming mode. (See Col. 6, lines 7 - 13 and 31 - 49.) Here it is understood that the 8th data bit of EEPROM 25's 16th byte is an HLOCK bit.

Referring to Claim 16, Urbas' transponder has means for generating a preamble to indicate the voltage level of signal received from the interrogator and transmitting the preamble to the interrogator. As shown in Fig. 1, the transponder has a detector 21 that provides direct current (DC) power to the transponder and detects a received signal's envelope, which is used to establish the PROG DATA signal (see Col. 4, lines 40 - 48). Because Urbas teaches that PROG DATA is low (or "0") when the supply voltage is less than three volts and high (or "1") when the supply voltage is greater than 3 volts (see Col. 8, lines 59 - 61), it is implied that detector 21 has a comparator. Urbas illustrates in Fig. 8 the transponder's preamble generator. If the transponder's supply voltage is greater than 3 volts, the preamble starts high and goes low (i.e., the first voltage indicator signal indicating PROG DATA's logic level of "1"). If the transponder's supply voltage is less than 3 volts, the preamble starts low and goes high (i.e., the second voltage indicator signal indicating PROG DATA's logic level of "0"). (See Col. 8, lines 39 - 67.)

Referring to Claim 41, Urbas teaches that a predetermined pulse sequence or a command signal places a transponder in the program mode and causes the transponder to receive and store data from the interrogator (see Col. 4, lines 26 - 28 and Col. 6, lines 22 - 24). Because Urbas also states that the waveform of the interrogator's signal can contain data and control information (see Col. 4, lines 9 - 10), it is understood that Urbas' command signal is pulse width modulated.

Regarding Claim 42, as shown in Fig. 1, Urbas' transponder has an EEPROM 25 that can be programmed to store data from the interrogator (see Col. 4. lines 26 - 28).

Regarding Claim 43, Urbas' transponder is able to send temperature data upon receiving a signal from the interrogator (see Col. 4, lines 9 - 10 and Col. 6, lines 61 - 66).

4. Claims 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Murdoch U.S. Patent No. 5,701,121.

Murdoch teaches that command signals can be sent to an actuator (i.e., "transponder") by modulating the magnetic field between the transponder and the base station (i.e., "interrogator") and that programming the memory of the transponder can also be performed by modulating the magnetic field with appropriate commands (see Col. 6, lines 19 - 25). Murdoch also states that pulse width modulation can be used (see Col. 5, lines 64 - 66).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 5, 9, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urbas et al. U.S. Patent No. 5,767,792, as applied to Claims 1, 7, and 13 above, and further in view of Carroll et al. U.S. Patent No. 5,517,194.

Regarding Claims 5, 9, 12, and 14, the status byte of Urbas' transponder lacks two seal bits that enables the transponder to be programmed if at least one of the seal bits is clear (i.e., logic "0") and a mode bit that prevents the address module from accessing the addresses in memory not corresponding to the mode indicated by the mode bit. In an analogous art, Carroll's passive transponder has four lock bits contained to word 0 of the non-volatile memory 48 (see Col. 17, lines 32 - 38). Carroll teaches that if bit 15 of word 0 (which corresponds to lock bit L0 in Fig. 4A) is logic 1, then all 16 rows (i.e., rows 0 - 15) of the memory are locked (see Col. 15, lines 25 - 29). If bit 14 of word 0 is (which corresponds to lock bit L1 in Fig. 4A) is logic 1, then only the status byte (i.e. word 0) is locked (see Col. 15, lines 44 - 46). Because Carroll teaches that a lock bit of word 0 cannot be changed once it is set (see Col. 17, lines 22 - 23), it is understood that bits 4 and 15 are seal bits. Carroll also imparts that various areas of memory 48 can be locked by setting bits 12 and 13. For example, if bit 12 (which corresponds to L3 in Fig. 4A) is logic 1 while bit 13 is logic 0, rows 1 - 5 of memory 48 are locked. If bit 12 is logic 0 while bit 12 while bit 13 is logic 1, then rows 1 - 3 of memory 48 are locked. If bits 12 and 13 are both logic 1, then rows 1 - 7 of memory 48 are locked. (See Col. 15, lines 37 - 44.) Here it is understood that bits 12 and 13 of the status byte are mode bits. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the status byte of Urbas' transponder as taught by Carroll, because a status byte with seal bits and

mode bits provides a user with better means for managing a memory device than a status byte with only one bit that is set to logic 1 to lock the entire contents of a memory device.

8. Claims 44 - 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urbas et al. U.S. Patent No. 5,767,792, as applied to Claim 1 above, and further in view of Young et al. U.S. Patent No. 5,978,192.

Regarding Claims 44 - 47, because Urbas discloses that passive transponder 100 in Fig. 9 - 12 includes a substrate 700 and a chip 710 that houses each of the transponder's structures including EEPROM 25, it is implied that Urbas' transponder is formed as an integrated circuit (see Col. 16, lines 40 - 46 and 52 - 57). Urbas teaches that detector 21 includes the necessary over-voltage protection for proper operation of the transponder (see Col. 4, lines 46 - 48). Because clamps limit the peak voltage of a semiconductor device and detector 21 is housed in chip 710, which is a semiconductor device, it is understood that detector 21 includes a semiconductor clamp to provide over-voltage protection. Urbas, though, is silent that the clamp is formed by a complementary metal-oxide semiconductor (CMOS) circuit. In an analogous art, Young teaches that clamp can be configured as a CMOS integrated circuit (see Figs. 3 and 4) or a bipolar integrated circuit (see Col. 1, lines 23 - 25). The clamp circuit in Fig. 4 has a CMOS inverter circuit 60 that comprises of an N-MOSFET 70 and a P-MOSFET 80. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the clamp of Urbas' transponder as taught by Young, because a CMOS integrated clamp circuit uses very little power.

CR

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clara Yang whose telephone number is (703) 305-4086. The examiner can normally be reached on 8:30 AM - 7:00 PM, Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

CY
December 23, 2002

TIMOTHY EDWARDS
PRIMARY EXAMINER